REMARKS

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached pages are captioned "**Version with Markings to Show Changes Made**."

No new matter has been introduced by any of the above amendments. In light of the above amendments and remarks, Applicants believe that Claims 1-29 are in condition for allowance, and allowance of the application is therefore requested.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as **first class mail** in an envelope addressed to: Commissioner for Patents, Washington, D.C., 20231, on October 3, 2002.

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Signature

VERSION WITH MARKINGS TO SHOW CHANGES MADE

CLAIMS

16. (New) A system, comprising:

a system backplane; and

a printed circuit board (PCB) inserted into the system backplane and coupled to receive power therefrom, the PCB comprising an integrated circuit that includes:

a first circuit that detects a hot swap condition during an insertion of the PCB into the system backplane when the system backplane is powered up;

a second circuit coupled to the first circuit that prevents a pn junction diode in a pull-up transistor from going into a forward bias condition; and

a third circuit coupled to the first and second circuits that prevents the pull-up transistor from turning on during the hot swap condition.

17. (New) The system of claim 16, wherein the first circuit detects a beginning and an ending of the hot swap condition.

18. (New) The system of claim 16, wherein the first circuit comprises a transistor having a gate coupled to an input/output voltage supply during the hot swap and further having a drain coupled to a pad that is coupled to a signal line of the system backplane during the hot swap.

19. (New) The system of claim 18, wherein the second circuit disconnects the NWELL of the pull-up transistor from the input/output voltage supply during the hot swap condition, providing isolation of the NWELL from the input/output voltage supply during the hot swap condition.

20. (New) The system of claim 19, wherein the second circuit further charges the NWELL to the voltage level of the signal line during the hot swap condition to prevent the pn junction diode from going into a forward bias condition.

21. (New) The system of claim 16, wherein the pull-up transistor is coupled to a pad of the integrated circuit.

22. (New) The system of claim 16, wherein the pull-up transistor is a PMOS transistor.

23. (New) A printed circuit board (PCB), comprising:

a plurality of power terminals; and

an integrated circuit coupled to the power terminals, the integrated circuit comprising:

a first circuit that detects a hot swap condition when power is applied to the power terminals;

a second circuit coupled to the first circuit that prevents a pn junction diode in a pull-up transistor from going into a forward bias condition; and

a third circuit coupled to the first and second circuits that prevents the pull-up transistor from turning on during the hot swap condition.

24. (New) The system of claim 23, wherein the first circuit detects a beginning and an ending of the hot swap condition.

25. (New) The system of claim 23, wherein the first circuit comprises a transistor having a gate coupled to an input/output voltage supply during the hot swap and further having a drain coupled to a pad that is coupled to a signal line of the PCB during the hot swap.

26. (New) The system of claim 25, wherein the second circuit disconnects the NWELL of the pull-up transistor from the input/output voltage supply during the hot swap condition, providing isolation of the NWELL from the input/output voltage supply during the hot swap condition.

27. (New) The system of claim 26, wherein the second circuit further charges the NWELL to the voltage level of the signal line during the hot swap condition to prevent the pn junction diode from going into a forward bias condition.

28. (New) The system of claim 23, wherein the pull-up transistor is coupled to a pad of the integrated circuit.

29. (New) The system of claim 23, wherein the pull-up transistor is a PMOS transistor.